REMARKS

Claims 1-20 were examined and reported in the Office Action. Claims 1-4, 11, 17 and 18 are rejected. Claims 5-10, 12-16, 19 and 20 are withdrawn from consideration. Claims 1-4, 11 and 17 are amended. Claims 1-20 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. Claims Rejected Under 35 U.S.C. 112

It is asserted in the Office Action that claim 1 is rejected under 35 U.S.C. § 112 second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has amended claim 1 to overcome the 35 U.S.C. § 112 second paragraph rejections.

II. Claims Rejected Under 35 U.S.C. 102(e)

It is asserted in the Office Action that claims 1-4 and 11 are rejected under 35 U.S.C. § 102(e), as being anticipated by U. S. Patent No. 6,578,145 issued to Hou ("Hou"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2131,

> '[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)).

Applicant's claim 1 contains the limitations of

> [a] data conversion/output apparatus comprising: a plurality of sensors; voltage-time conversion circuits which are arranged adjacent to said respective plurality of sensors and change output levels upon the lapse of times corresponding to output voltage values from said plurality of sensors after a conversion operation start point in order to convert voltage outputs of said plurality of sensors into times; and sensed data generation circuits for outputting, as digital data, lapse times until the output levels of said voltage-time conversion circuits change after a conversion start point, said sensed data generation circuits each include a counter for counting a clock signal, wherein an operation start of the voltage-time conversion circuits and a start of count operation of the counter are staggered.

Hou discloses an image sensor that converts light intensity signals to digital signals without using A/D converters. Distinguishable, In Applicant's claimed invention the voltage-time conversion circuit changes its output level after a time corresponding to output voltage, which is analog data output from the sensor, has lapsed from a predetermined conversion operation start point of time and outputs one bit digital data. This enables long-distance propagation of a signal as one digital signal of H level or L level via a data bus. Therefore, precision of the data is prevented from being degraded. Additionally, Applicant's claimed invention (see Applicant's specification, the seventh embodiment at pages 21-22) easily realizes conversion precision adjustment corresponding to sensitivity adjustment of the A/D converter, and effectively uses the data width of output data. Moreover, Hou does not teach, disclose or suggest "said sensed data generation circuits each include a counter for counting a clock signal, wherein an operation start of the voltage-time conversion circuits and a start of count operation of the counter are staggered."

Therefore, since Hou does not disclose, teach or suggest all of Applicant's amended claim 1 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(e) has not been adequately set forth relative to Hou. Thus, Applicant's amended claim 1 is not anticipated by Hou. Additionally, the claims that directly or indirectly depend on claim 1, namely claims 2-4 and 11, are also not anticipated by Hou for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 102(e) rejections for claims 1-4 and 11 are respectfully requested.

III. Claims Rejected Under 35 U.S.C. 103(a)

It is asserted in the Office Action that claims 17 and 18 are rejected in the Office Action under 35 U.S.C. § 103(a), as being obvious over "*A Digital Camera for Machine Vision*", Conference on Industrial Electronics, Control and Instrumentation, 1994, by A. Simoni et al ("Simoni"), in view of Hou. Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2142

> [t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Further, according to MPEP §2143.03,

> [t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). *All words in a claim must be considered* in judging the patentability of that claim against the prior art. (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's claim 17 contains the limitations of

> [a] data conversion/output apparatus comprising: a column decoder for selecting at once a plurality of pixels aligned on an arbitrary column from pixels arrayed in a matrix; a plurality of data buses each commonly connected to a plurality of pixels aligned on each

> row out of the pixels; a counter for sequentially outputting count values in accordance with internal count operation; a plurality of latch circuits which are arranged on respective rows and latch the count values from said counter in accordance with level changes of said data buses corresponding to the respective rows; a row decoder for selecting a row having a desired pixel out of the pixels selected by said column decoder; and a plurality of row switches which are arranged on the respective rows and output as sensed data of desired pixels the count values latched by said latch circuits corresponding to the respective rows, wherein each of the pixels has a sensor for outputting a detection result as an output voltage value, a voltage-time conversion circuit for changing an output level upon the lapse of time corresponding to an output voltage value from said sensor after a predetermined conversion operation start point, and a column switch for outputting in accordance with selection of a pixel by said row decoder an output from said voltage-time conversion circuit to a data bus connected to the pixel, and an operation start of the voltage-time conversion circuit and a start of count operation of the counter are staggered.

Simoni discloses a digital camera to be used in machine vision applications. Hou discloses an image sensor that converts light intensity signals to digital signals without using A/D converters. In Applicant's claimed invention, however, the voltage-time conversion circuit changes its output level after a time corresponding to output voltage, which is analog data output from the sensor, has lapsed from a predetermined conversion operation start point of time and outputs one bit digital data. This enables long-distance propagation of a signal as one digital signal of H level or L level via a data bus. Therefore, precision of the data is prevented from being degraded. Additionally, Applicant's claimed invention easily realizes conversion precision adjustment corresponding to sensitivity adjustment of the A/D converter, and effectively uses the data width of output data. Moreover, neither Simoni, Hou, and therefore, nor the combination of the two teach, disclose or suggest "said voltage-time conversion circuit to a data bus connected to the pixel, and an operation start of the voltage-time conversion circuit and a start of count operation of the counter are staggered."

Neither Simoni, Hou, and therefore, nor the combination of the two, teach, disclose or suggest the limitations contained in Applicant's amended claim 17, as listed above. Since neither Simoni, Hou, and therefore, nor the combination of the two, teach, disclose or suggest all the

limitations of Applicant's amended claim 17, Applicant's amended claim 17 is not obvious over Simoni in view of Hou since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claim that directly depends from amended claim 17, namely claim 18, would also not be obvious over Simoni in view of Hou for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claims 17 and 18 are respectfully requested.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-20 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: May 10, 2006

By: _____
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on May 10, 2006.

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Jean Svoboda